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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/531,134	04/13/2005	Adnan Al-Adnani	AAT-102US	5098

23122 7590 06/08/2009

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EXAMINER	
SMITH, JOSHUA Y	
ART UNIT	PAPER NUMBER
2419	
MAIL DATE	DELIVERY MODE
06/08/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/531,134	AL-ADNANI, ADNAN	
	Examiner	Art Unit	
	JOSHUA SMITH	2419	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 January 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The amendment filed 01/15/2009 has been entered.

- **Claims 1 and 3-11 are pending.**
- **Claim 2 is previously cancelled.**
- **Claims 1 and 3-11 stand rejected.**

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1 and 3-7, 9, 11 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1 and 9 each state "Reconfigurable signal processing **architecture** comprising" modules (emphasis added by examiner). The specification states in page 6, lines 5-7, 2nd paragraph, "The proposed **architecture** can be realized in **software** or hardware depending on the computational complexity, power requirements of the system." (emphasis added). As a result, the architecture comprising modules of Claim 1 is completely software, and the architecture comprising modules of Claim 9 is completely software, and this causes Claims 1 and 9 to be directed toward software, which is non-statutory subject matter and where software does not define any structural and functional interrelationships between the software and other claimed aspects of the invention which permit the functionality of the software to be realized.

Claims 3-7 and 11 are rejected through dependence from Claim 1.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Markwalter et al. (Patent No.: US 6,577,630 B1) in view of Tan et al. (Pub. No.: US 2004/0202179 A1), hereafter respectively referred to as Markwalter and Tan.

In regard to Claim 1, Markwalter teaches in column 8, line 65 to column 9, line 12, and in FIG. 2 and FIG. 3, a frame control FEC decoder 64 (FIG. 2) receives coded frame control information (item 98, FIG. 3) from an FFT 58 (FIG. 2), and the frame control FEC decoder 65 (FIG. 2) uses these inputs to decode and demodulate the frame control information in a frame delimiter (item 92, FIG. 3), and once decoded and demodulated, the frame control information (item 98, FIG. 3) is passed to a MAC interface unit 74 (FIG. 2) for transfer to a MAC unit, and the MAC unit determines from the information if the delimiter (item 92, FIG. 3) indicates a start-of-frame, and if a start-of-frame is indicated, a RX configuration unit (item 72, FIG. 2) receives from the MAC unit frame control information to indicate that further decoding is necessary and the RX configuration unit uses the frame control information to direct the controller to configure the receiver units (items 66 and 68, FIG. 2) for further decoding of the remainder of the frame, such as a payload (item 82, FIG. 3) (a plurality of reconfigurable data processing modules, a single decoder serving a plurality of modules, a single decoder decoding bits of packets and providing respective signals to a plurality of modules, in which a portion of a packet is used to change data processing performed by a module, data portion of a

packet is processed by a data processing module responsive to a respective selection signal).

Markwalter fails to teach data is input to a plurality of modules in a packet frame structure including configuration frames and processing frames, each frame including a header section and a data section, a header section having at least one mode selection bit indicating whether the data section of the frame contains reconfiguration data or processing data, a single decoder serving a plurality of modules, the single decoder decoding the mode selection bits of the packets, wherein each module is operable in a reconfiguration mode in which a data portion of a packet is used by a module to change data processing performed by the module.

Tan teaches in paragraphs [0071] and [0072], a configuration ATM cell (a packet frame structure) is a special ATM cell (including configuration frames and processing frames) such as an unassigned ATM cell in which all bits in the ATM header are zero (a header section giving at least one mode selection bit indicating whether the data section of the frame contains reconfiguration data or processing data), or a system specified ATM cell, and where a configuration ATM cell can be generated by a system host processor, and it carries configuration control information in its payload, and where a configuration ATM cell can be sent to a UTOPIA extension device from an ATM layer device or a PHY layer device through their UTOPIA interfaces, and upon receipt of a configuration cell, a link control of the UTOPIA extension device send a configuration information to a configuration register (a single decoder) which, in turn, forwards the information to all elements (modules) of the device which need to be configured (each

module is operable in a reconfiguration mode in which a data portion of a packet is used by a module to change data processing performed by the module) (data is input to a plurality of modules in a packet frame structure including configuration frames and processing frames, each frame including a header section and a data section, a header section having at least one mode selection bit indicating whether the data section of the frame contains reconfiguration data or processing data, a single decoder serving a plurality of modules, the single decoder decoding the mode selection bits of the packets, wherein each module is operable in a reconfiguration mode in which a data portion of a packet is used by a module to change data processing performed by the module).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the invention of Tan with the invention of Markwalter since Tan provides an apparatus for extending the transmission range of UTOPIA ATM and UTOPIA packet interfaces, extending the transmission range of UTOPIA interfaces which maintain compatibility with the existing standards, and for extending the transmission range of UTOPIA interfaces which enable communication via a "transmission cloud" (see Tan, paragraphs [0023]-[0026]), which can be introduced into the system of Markwalter to have compatibility with UTOPIA and ATM and allow packets to be transmitted over extended transmission ranges between network components, increasing flexibility for the arrangement of the system of Markwalter.

Claims 3, 4, 6, 7 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Markwalter in view of Tan, and further in view of Laufer et al. (“PCI-

PipeRench and the SwordAPI: A System for Stream-based Reconfigurable Computing", 1999, IEEE Comput. Soc., US, p. 303), hereafter referred to as Laufer.

In regard to Claim 3, as discussed in the rejection of Claim 1, Markwalter in view of Tan teaches a frame header, a mode selection bit, and a module.

Markwalter fails to teach a bit for each module.

Laufer teaches in page 203, lower half of first column, a Chip ID tells each chip whether to keep a header or pass it along.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the invention of Laufer with the invention of Markwalter since Laufer provides a technique where a component can determine if it is required to process a packet or pass it to another component, prevent unnecessary processing and reducing processing time of the system of Markwalter.

In regard to Claim 4, as discussed in the rejection of Claim 4, Markwalter in view of Tan and Laufer teaches mode selection bit of a frame header.

Markwalter teaches in column 8, line 65 to column 9, line 12, and in FIG. 2 and FIG. 3, a frame control FEC decoder 64 (FIG. 2) receives coded frame control information (item 98, FIG. 3) from an FFT 58 (FIG. 2), and the frame control FEC decoder 65 (FIG. 2) uses these inputs to decode and demodulate the frame control information in a frame delimiter (item 92, FIG. 3), and once decoded and demodulated, the frame control information (item 98, FIG. 3) is passed to a MAC interface unit 74 (FIG. 2) for transfer to a MAC unit, and the MAC unit determines from the information if

the delimiter (item 92, FIG. 3) indicates a start-of-frame, and if a start-of-frame is indicated, a RX configuration unit (item 72, FIG. 2) receives from the MAC unit frame control information to indicate that further decoding is necessary and the RX configuration unit uses the frame control information to direct the controller to configure the receiver units (items 66, 68, and 70, FIG. 2) for further decoding of the remainder of the frame, such as a payload (item 82, FIG. 3) (a single decoder decodes a frame header to provide respective signals to a plurality of modules).

In regard to Claim 6, as discussed in the rejection of Claim 1, Markwalter in view of Tan teaches modules and mode selection signals.

Markwalter fails to teach modules are connected to each other in series.

Laufer teaches in page 203, lower half of first column, a number of reconfigurable chips chained together, where the output of each chip is connected directly to the input of the next one (modules are connected to each other in series).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the invention of Laufer with the invention of Markwalter since Laufer provides a technique where a component can determine if it is required to process a packet or pass it to another component, prevent unnecessary processing and reducing processing time of the system of Markwalter.

In regard to Claim 7, as discussed in the rejection of Claim 1, Markwalter in view of Tan teaches modules, incoming data, and a header.

Markwalter fails to teach a bypass mode where data is not acted on by a module and where a header indicates this.

Laufer teaches in page 203, lower half of the first column to the upper half of the second column, a Chip ID field of a header tells each chip whether to keep the header or pass it along, and when an input controller receives a bare packet, it checks to see if it is currently processing a header, and, if not, the packet must be for a device further on the chain, and the packet is passed on untouched (teach a bypass mode where data is not acted on by a module and where a header indicates this).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the invention of Laufer with the invention of Markwalter since Laufer provides a technique where a component can determine if it is required to process a packet or pass it to another component, prevent unnecessary processing and reducing processing time of the system of Markwalter.

In regard to Claim 11, as discussed in the rejection of Claim 1, Markwalter in view of Tan teaches modules, incoming data, and a header.

Markwalter fails to teach a bypass mode where data is not acted on by a module and where a header indicates this.

Laufer teaches in page 203, lower half of the first column to the upper half of the second column, a Chip ID field of a header tells each chip whether to keep the header or pass it along, and when an input controller receives a bare packet, it checks to see if it is currently processing a header, and, if not, the packet must be for a device further on

the chain, and the packet is passed on untouched (teach a bypass mode where data is not acted on by a module and where a header indicates this).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the invention of Laufer with the invention of Markwalter since Laufer provides a technique where a component can determine if it is required to process a packet or pass it to another component, prevent unnecessary processing and reducing processing time of the system of Markwalter.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Markwalter in view of Tan, Laufer, and further in view of Griffin et al. (Patent Number: 5,406,403), here after referred to as Griffin.

In regard to Claim 5, as discussed in the rejection of Claim 1, Markwalter in view of Tan teaches that decoded mode selection data is supplied to modules.

Markwalter fails to teach data is supplied in parallel.

Griffin teaches in column 4, lines 9-12, rearranging serial data into parallel data (signals are supplied in parallel).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the invention of Griffin with the invention of Markwalter since Griffin provides a method of forwarding data in parallel, which can be faster in certain cases than forwarding data in serial.

Claims 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Markwalter in view of Tan, and further in view of Chieu et al. (Patent No.: US 6,501,807 B1), hereafter referred to as Chieu.

In regard to Claim 8, as discussed in the rejection of Claim 1, Markwalter in view of Tan teaches digital processing and digital components that are configurable and the architecture of Claim 1.

Markwalter fails to teach a radio signal processing apparatus where signals are processed digitally.

Chieu teaches in column 3, lines 45-47, a digital signal processor (DSP) and a radio module (a radio signal processing apparatus where signals are processed digitally).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the invention of Chieu with the invention of Markwalter since Chieu provides an apparatus with components that can allow wireless digital communications, which can be used to extend the apparatus of Markwalter to include wireless services to customers, such as cellular or WiMAX services.

In regard to Claim 10, as discussed in the rejection of Claim 8, Markwalter in view of Tan and Chieu teaches a signal processing apparatus.

Markwalter fails to teach a radio signal processing apparatus selected from a group consisting of a receiver, a transmitter, or a transceiver.

Chieu teaches in column 2, line 66 to column 4, line 6, and in FIG. 1, Sheet 1 of 6, a transmitter portion, a receiver portion, and a hybrid (a group consisting of a receiver, a transmitter, or a transceiver).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the invention of Chieu with the invention of Markwalter since Chieu provides an apparatus with components that can allow wireless digital communications, which can be used to extend the apparatus of Markwalter to include wireless services to customers, such as cellular or WiMAX services.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Markwalter in view of Tan and Williams (Patent No.: US 6,775,283 B1), hereafter referred to as Williams.

In regard to Claim 9, Markwalter teaches in column 8, line 65 to column 9, line 12, and in FIG. 2 and FIG. 3, a frame control FEC decoder 64 (FIG. 2) receives coded frame control information (item 98, FIG. 3) from an FFT 58 (FIG. 2), and the frame control FEC decoder 65 (FIG. 2) uses these inputs to decode and demodulate the frame control information in a frame delimiter (item 92, FIG. 3), and once decoded and demodulated, the frame control information (item 98, FIG. 3) is passed to a MAC interface unit 74 (FIG. 2) for transfer to a MAC unit, and the MAC unit determines from the information if the delimiter (item 92, FIG. 3) indicates a start-of-frame, and if a start-of-frame is indicated, a RX configuration unit (item 72, FIG. 2) receives from the MAC unit frame control information to indicate that further decoding is necessary and the RX

configuration unit uses the frame control information to direct the controller to configure the receiver units (items 66 and 68, FIG. 2) for further decoding of the remainder of the frame, such as a payload (item 82, FIG. 3) (a reconfigurable data processing module in which data is input to a module in a packet frame structure, wherein a module is operable in a reconfiguration mode responsive to a frame portion).

Markwalter fails to teach a packet frame structure including configuration frames and processing frames, each frame including a header having at least one mode selection bit indicating whether a frame contains reconfiguration data or processing data, and wherein a module is operable in a reconfiguration mode or a processing mode responsive to a frame header and mode selection bits are separated from data in each frame and are used to control mode selection logic in a module for determining how incoming data is handled.

Tan teaches in paragraphs [0071] and [0072], a configuration ATM cell (a packet frame structure) is a special ATM cell (including configuration frames and processing frames) such as an unassigned ATM cell in which all bits in the ATM header are zero (a header section giving at least one mode selection bit indicating whether the data section of the frame contains reconfiguration data or processing data), or a system specified ATM cell, and where a configuration ATM cell can be generated by a system host processor, and it carries configuration control information in its payload, and where a configuration ATM cell can be sent to a UTOPIA extension device from an ATM layer device or a PHY layer device through their UTOPIA interfaces, and upon receipt of a configuration cell, a link control of the UTOPIA extension device send a configuration

information to a configuration register (a single decoder) which, in turn, forwards the information to all elements (modules) of the device which need to be configured (each module is operable in a reconfiguration mode in which a data portion of a packet is used by a module to change data processing performed by the module) (a packet frame structure including configuration frames and processing frames, each frame including a header having at least one mode selection bit indicating whether a frame contains reconfiguration data or processing data, and wherein a module is operable in a reconfiguration mode or a processing mode responsive to a frame header and mode selection bits are separated from data in each frame and are used to control mode selection logic in a module for determining how incoming data is handled).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the invention of Tan with the invention of Markwalter since Tan provides an apparatus for extending the transmission range of UTOPIA ATM and UTOPIA packet interfaces, extending the transmission range of UTOPIA interfaces which maintain compatibility with the existing standards, and for extending the transmission range of UTOPIA interfaces which enable communication via a "transmission cloud" (see Tan, paragraphs [0023]-[0026]), which can be introduced into the system of Markwalter to have compatibility with UTOPIA and ATM and allow packets to be transmitted over extended transmission ranges between network components, increasing flexibility for the arrangement of the system of Markwalter.

Markwalter fails to teach default data supplied from memory outside a module.

Williams teaches in column 8, lines 16-36, and in FIG. 2-1 and FIG. 2-2, a network interface controller 251 (FIG. 2-1 and FIG. 2-2) (a module) includes an expansion bus interface unit 242 interfaces to nonvolatile (e.g., EPROM 252 (FIG. 2-1) or Flash memory) storage (memory outside a module) for boot programming (default data) used during startup (default data supplied from memory outside a module).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the invention of Williams with the invention of Markwalter since Williams provides a system where boot programming is located external to a module, which can be introduced into the system of Markwalter to allow a module to contain volatile memory, which allows faster processing speeds, and to load necessary programming from an external memory upon startup or anytime new programming is needed.

Response to Arguments

Applicant's arguments with respect to claims 1 and 3-11 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOSHUA SMITH whose telephone number is (571)270-1826. The examiner can normally be reached on Monday-Friday, 10:30am-7pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chirag Shah can be reached on (571)272-3144. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Joshua Smith
/J.S./
Patent Examiner
04 June 2009

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